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# Stacked and Doherty Power Amplifier for 6G Communication Deployment

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**Abstract**
This paper presents a fully integrated stacked architecture to address the challenges of 6G application using CMOS analog pre-distortion and tunable neutralization techniques. By using this method for the stacked power amplifier design, a baseband and passband impedance transformation is achieved, that combined with the stacked power amplifier architecture allows for high efficiency in deep back off, with a reduced load modulation for high bandwidth. This project designs an efficient Stacked Power Amplifier (PA) for 6G. The power amplifier is implemented in 180nm CMOS technology using Cadence and ADS tool. The usage of a diode pre-distorter for analog pre-distortion is investigated for the stacked power amplifier design. It is shown that the linearity of the stacked power amplifier has been significantly improved compared to a bipolar transistor at almost no additional layout size. This research work presents design of a Ka band power amplifier for sixth generation (6G) mobile communication in CMOS design. The stacked power amplifier consists of two different stages of architecture. With 5-volt supply, the stacked power amplifier achieves a small-signal gain of 16 dB, saturated output power ($P_{sat}$) of 18 dBm, and achieves the maximum power added efficiency of 34.79%. The amplifier has been designed in 180-nm CMOS technology.

**Keywords:** CCLNA, Power Amplifier, Conversion gain, Saturated Output Power, CMOS technology.

## 1. INTRODUCTION

Due to the numbers of users and great demand in downloading and uploading content there has been a extreme increase in the use of smart phones in the recent years. Since mobile users are expecting more data speed and secure service for the current technology, these 4G and 5G cannot be supported. This technology will impact following mobile communications system, 100x more storage, Higher data speed, Higher frequency, high service providers etc.

Due to usage of high data used by the current users, the service providers have a problem with the current RF band. To overcome this 5G technologies will provide a new spectrum that has not been used before. Since 4G networks operates at less GHz downloading and uploading data is lower. To overcome this 5G technology is expected to operate at a frequency of more than 100GHz. The millimeter wave spectrum shows the possible of giving thousands of times of more data in a future wireless communication [1]. The large amount of power in the transmitter are being consumed by the power amplifier. Due to limited efficiency and dynamic range in the power amplifier, high power is consumed, and the power amplifier gives a linear behavior [2-3].

5G applications are studied because of their low cost and functionality. 5G technology for recent years shown the need for highly linear and effective power amplifier in order to give high data rate [4]. More CMOS design is possible in order to control the power output drawn on the current and the circuit voltage. In addition, output power needs linearity circuit. In wireless communication systems Power amplifier (PA) plays a major role in it. The power amplifier output power required is as high as possible for a Long Communication Systems. Due to less breakdown voltage, the power amplifier in CMOS has low saturated output power. To improve the power amplifier status, transformer based differential design for output sequence is preferred [5].

In this paper, Ka band CMOS power amplifier design and theoretical values are presented. The improved design and waves for high frequency and high power added efficiency are given. The simulation results the large signal performance and small signal gain results. The remaining paper is organized as follows. Part 2 describes existing works on stacked

power amplifier identification. Part 3 presents the circuit designs and analysis of AC and DC power sources. Part 4 reports the analytical and theoretical values of the circuit. Part 5 discusses the significance of the observed findings. Part 6 concludes this paper.

## 2. PROPOSED DESIGN

### 2.1. Stacked Power Amplifier

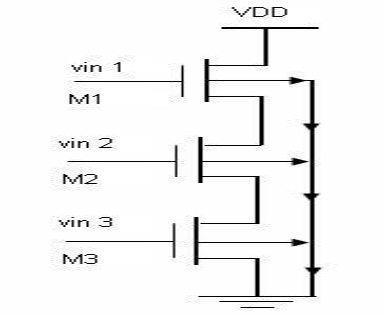



**Fig. 1** Stacked power amplifier

In wireless communication system, Power amplifier plays an important role in it. There are different types of power amplifiers among, stacked power amplifier is one of the technologies which has high gain and frequency [6-9]. Stacked technique is nothing but series of transistors are arranged, with input are given in the one end and output are taken by the other end. Capacitance acts a rectifying element to this stacked power amplifier. It isolates the input signal and biasing voltage. Since the input signal is applied to this transistor via this coupling transistors. The uses of power amplifier are, it increases the high input power level and produce the required output power with fast switching [10-13]. In multicell stacked devices this series input configuration plays an important role. In base station the RF power signals are boosted by this power amplifier. It was based on two technologies; one is silicon based and another one is Diffused Metal oxide semiconductor or RF gallium nitride. Generally, the 3G base stations are based on LDMOS. These LDMOS are highly inexpensive due to this they took nearly a year to implement in 4G. In base stations these power amplifiers play an important role in converting a low power RF signal into a very high-power signal [14-18]. In the base station not only the power amplifier used and there are many devices based on their various process.

### 2.2 Circuit Design and Implementation

Design Implementation: In this paper, AC and DC analysis of stacked power amplifier techniques are designed and analyzed. Envelop Tracking (ET) is the first CMOS power amplifier which was designed and used in wireless communication transmitters in order to improve the power added efficiency and the signal gain. DC analysis of stacked amplifier is shown in fig.3. In DC analysis bipolar transistors are replaced with CMOS design and measured the input and output power and also attain the frequency of operation at 5GHz with power added efficiency of 34%. In AC analysis the power amplifier attains the overall signal gain of 18dB with output power saturated of dBm, and it operates at the frequency of 5GHz. This entire circuit design was using LTspice platform in 180 nm technology.

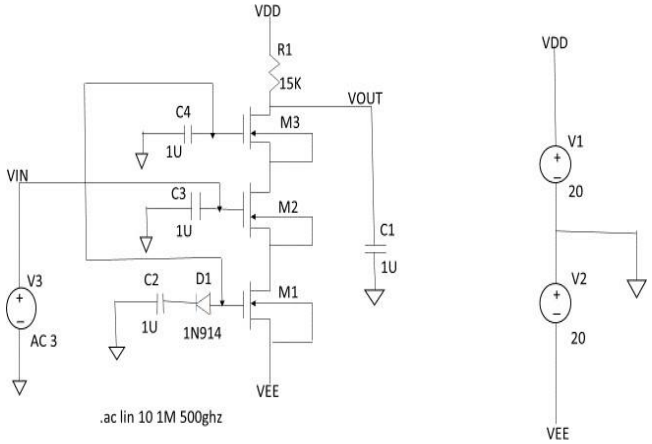



**Fig. 2** AC analysis circuit

Pre-Distortion: Basically, pre-distortion techniques have classified into two types, which was analog and digital. Less than 20 GHz applications are used by digital pre-distortion. Because of this it operates at less frequency and power consumption is less when compared to analog pre-distortion. In digital pre-distortion large baseband bandwidth operates at high clock rate. Normally in power amplifiers the operating frequency and high data speed are attain only in analog pre-distortion. The designed proposed power amplifier carried out one biasing scheme i.e., diode pre- distorter which was nothing but an analog pre-distortion. By using diode pre-distorter, it produces higher output power with lower input terminals and also produce a better linearity signal. The word distortion is nothing, but it denotes the shape of things. For example, audio signal is being represented by sound and video signal is being represented by images.

AC Analysis: In wireless communication, power amplifier plays an important role. Required output power is generated by increasing the input power level. In this paper, we have designed a stacked power amplifier using analog pre-distortion technique in CMOS to improve signal gain and the Power added efficiency of the amplifier.

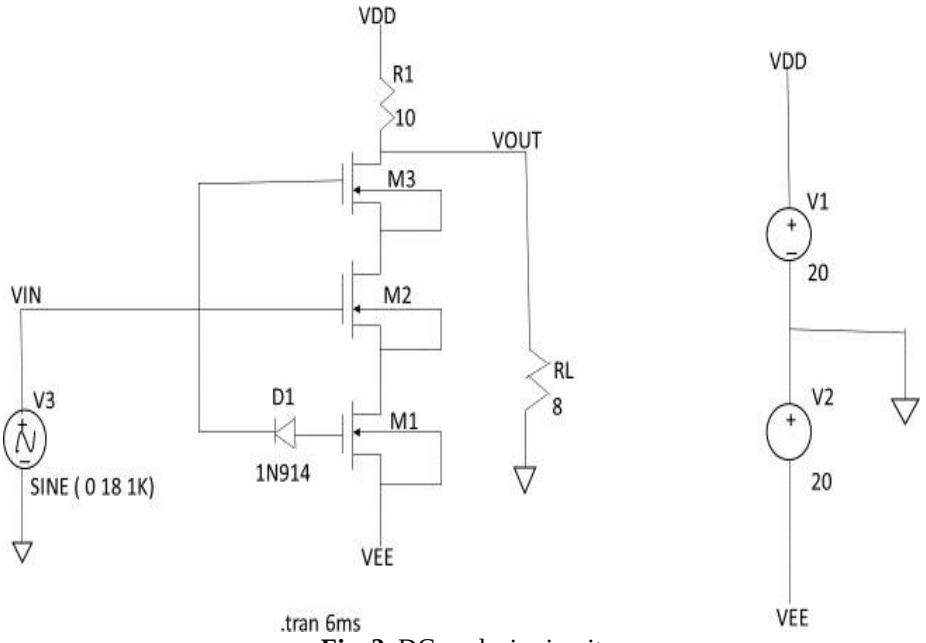



**Fig. 3** DC analysis circuit

Figure 2 Shows the circuit design of AC designed stacked power amplifier which was designed using in 180 nm technology. The input amplitude of this circuit is around 3V. The capacitor is connected in series to isolate the input signal and biasing voltage. The output of power amplifier normally driven by very low impedance network mostly consider as speaker, speaker is connected in the form capacitance c1 respectively. As the power increases in the input, the rectified dc current of the diode increases.

Gain-compression and phase distortion of circuit improves due to diode pre distorter which acts as an analog pre-distortion. In this designed power amplifier, bipolar transistors are being replaced with CMOS design technique. It increases the power added efficiency. When we apply input signal to CMOS, it should not affect the biasing condition of CMOS, similarly the biasing voltage should not affect the input signal, to isolate the input signal and biasing voltage. Thus, coupling capacitor is used, in other words, the input signal is applying to CMOS via this coupling capacitor in ac analysis. This designed power amplifier gives the overall the signal gain of greater than 16dB, and saturated output power pf 18dBm. This proposed design consumes less power, less heat generation and more stability as compared to bipolar transistor. This proposed stacked power amplifier operates between the frequencies of 30-GHz.

DC ANALYSIS: The proposed DC circuit design was shown in figure 3. In this design also bipolar transistors are replaced with MOS transistors. The bias networks are used as MOS transistors in order to improve the signal and power added efficiency. In this design the dual power supply is connected, Due to this that the output swing is almost doubled. We have given the sinusoidal input and the sine wave amplitude that is input amplitude around 18V and frequency around 1k and the output of the power amplifier is normally driven by the very low impedance network. Mostly let's consider output load might be a speaker, so speaker is represented in the form of resistance [RL] over here. For AC signal these capacitor acts as a short circuit. In this small signal equivalent model for CMOS, first consider all the dc sources as zero and replace the coupling and bypass capacitor with short circuit.

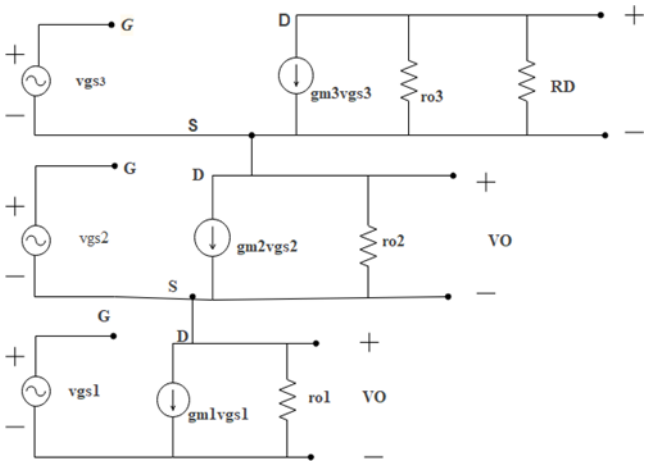



**Fig. 4** AC equivalent circuit of proposed stacked power amplifier

Figure 4 shows the AC equivalent circuit of stacked power amplifier. As you aware the capacitor blocks dc signal, because for dc signal it will act as an open circuit. The operating frequency of capacitor for DC voltage is zero and the reactant of capacitor is infinity.

Voltage Gain of The Circuit: "Amplification" of an amplifier is measured by the gain of an amplifier. For example, by using we can calculate the voltage gain, current gain, power gain how much increase in the amplitude of a signal". From the above AC equivalent circuit, the voltage gain of circuit is derived below

$V_{01} = -g_{m1}V_{gs1}$ ($V_{gs1}$ is equal to $V_i$) $V_{01} = -g_{m1}(V_i)$ (1)

$V_{02} = -g_{m2}V_{gs2}$ ($V_{gs2}$ is equal to $V_i$) $V_{02} = -g_{m2}(V_i)$ (2)

$V_{03}/R - V_{02}/R - V_{01}/R + g_{m2}V_{gs2} + g_{m1}V_{gs1} = 0$

$V_{03}/R - V_{02}/R = V_{01}/R + g_{m2}V_{gs2} + g_{m1}V_{gs1} = 0$

$V_{03}/R = 1/R + g_{m2}(-g_{m1}(V_i) + g_{m1}V_{gs1} + V_{02})V_{03}/R = -g_{m1}r(g_{m2})$

$A_V = -(g_{m1}r)(g_{m2}r)(g_{m3}r)$ (3)

This result can be derived from the $m_1.m_2,m_3$ changes an input voltage $\Delta V_{in}$ to a drain current change $(g_{m1})(g_{m2})(g_{m3})\Delta V_{in}$ and hence an output voltage change $-(g_{m1})(g_{m2})(g_{m3})R\,\Delta V_{in}$ . Since $g_m$ itself varies with the input signal according to $g_m = \mu_n C_{ox}(w/l)(V_{GS} - V_{TH})$, If the signal is large, then the gain of the circuit changes significantly. When $V_{in}$ increases the channel length modulation is neglected and $V_{out}$ drops high and in saturation point the transistor continues to operate until $V_{in}$ exceed $V_{out}$ and by $V_{th}$. $V_{out} << 2(V_{in} - V_{TH})$, and from the equivalent circuit of figure 4.

Theoretical value of the voltage gain achieved 16dB, 18 dBm Bandwidth (BW) 30- GHz (80%) with 18dBm of maximum Saturated output power and with maximum power added efficiency of 34.86%.

## 3. SIMULATION RESULTS

Figure 5 to 8 shows the validation of stacked power amplifier, which was simulated using 180 nm CMOS technology. Presenting good input matching and gives the small signal gain of 16 dB , this stacked power amplifier shows a measured ($P_{sat}$) power of 18 dBm, frequency at 30-GHz and with maximum power added efficiency of 34.86%.

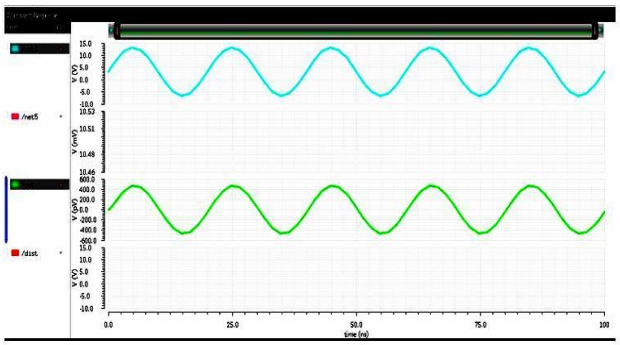


**Fig. 5** AC analysis

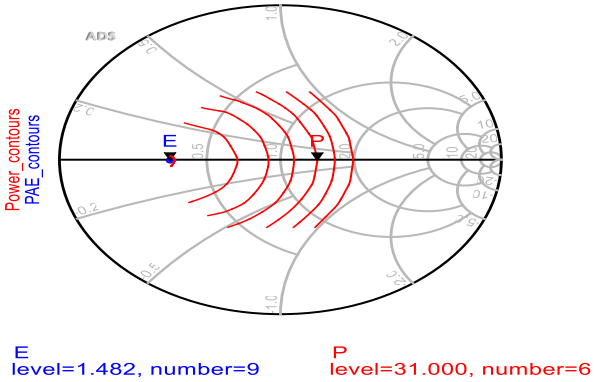



**Fig. 6** Power contours

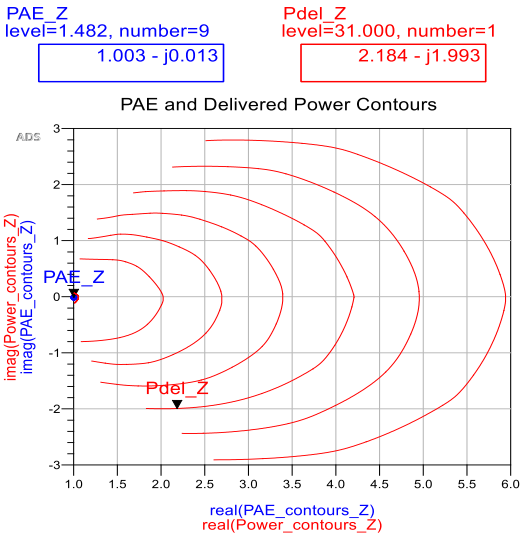
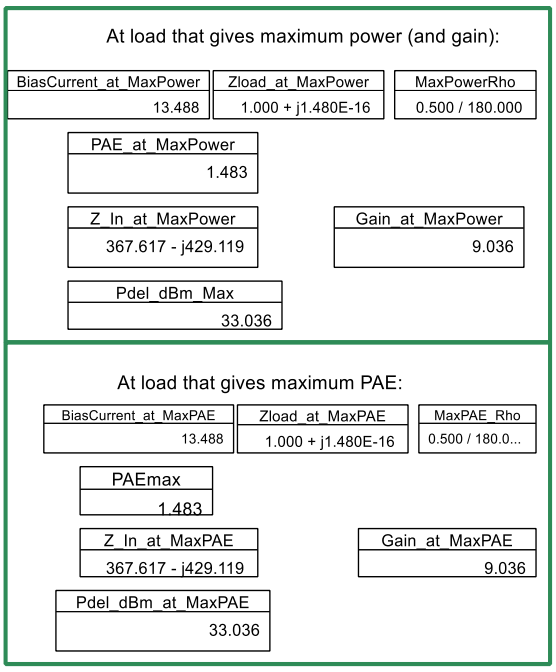



**Fig. 7** Power added efficiency



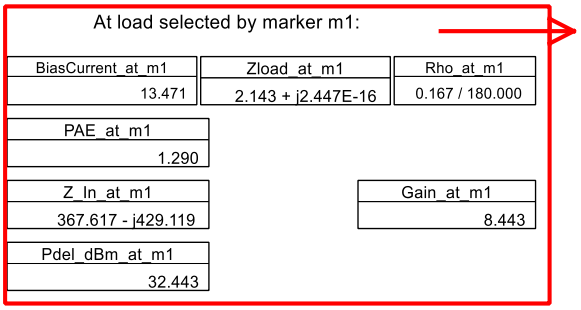



**Fig. 8** Power and Gain illustrations

**Table 1** Performance comparison with various power amplifiers for 5G CMOS

| **Parameters** | **Our Work** | **[1]** | **[2]** | **[3]** | **[4]** |
|---|---|---|---|---|---|
| Technology | 180 nm CMOS | 130 nm CMOS | 180 nm CMOS | 130 nm SiGe | 60 nm CMOS |
| Frequency(GHz) | 30 | 28 | 2.8 | 24 | 32 |
| PAE(max) % | 34.79 | 26 | 25.54 | 35 | 32.9 |
| ($P_{sat}$) power(dBm) | 18 | 16 | 7.05 | 18.6 | 15.3 |
| Gain (dB) | 16 | 14.6 | 7.17 | 15 | 12.9 |
| $V_{dd}$(V) | 5 | 5.5 | 5 | 4 | 1.1 |

## 4. CONCLUSIONS AND FUTURE SCOPE

In this paper, the proposed design of DPA using a 0.18µm CMOS technology at millimeter Wave frequency is presented. Design, analysis, and simulation results have been provided. Simulated results show the overall signal gain, and power added efficiency of power amplifier has been increased by 34.79%. Power amplifier performances can be improved by selecting an optimal capacitance. Linearity and Efficiency is improved at higher frequencies. This paves way for enhancement of Power amplifier for Nano-satellite applications and 6G deployment.

## REFERENCES

1. D.Y.C. Lie, “RF-SOC: Integration trends of on-chip CMOS power amplifier benefits of external PA versus Integrated PA for portable wireless communications”, International Journal of Microwave Science and Technology, Vol 20, No 10,pp 380- 390, 2021.
2. R.Eskandari et all, “ A wide band noise cancelling balun LNA employing current reuse technique’’ Microelectronics Journal (76) 1-7, Feb 2020.
3. F. Zhang and P.R. Kinget, “Low-Power programmable gain CMOS distributed LNA and PA” IEEE Journal of Solid-State Circuits, vol.41, No.6, pp.1333-1343, Jun. 2019.
4. R.E. Mclntosh, “A millimeter Wave Cloud RADAR profiling system”, Proceedings of IGARSS, IEEE International Geoscience and Remote Sensing Symposium, 8-12 Aug, 2022.
5. S.C. Shinetal, “A 24GHz,3.9dB NF Low Noise amplifier using 180nm CMOS technology”, IEEE Microwave and Wireless component letters, Vol 15,No 7, pp 448-450, July 2015.
6. Kim J, Hoyos Sand Silva-Martinez J. “Wideband common-gate CMOS LNA employing dual negative feedback with simultaneous noise, gain, and bandwidth optimization”, IEEE Transactions on Microwave Theory and Techniques, Vol. 58, pp.2340-2351. 2019.
7. E. Bloch and E. Socher, “Beyond the Smith chart: A universal graphical tool for impedance matching using transformers,” IEEE Microw. Mag., Vol.15, no.7, pp.100-109, Dec. 2017.
8. Rashtian H , Mirabbasi S , Taris T , Deval Y and Begueret J B A 4-stage 60-GHz low-noise amplifier in 65-nm CMOS with body biasing to control gain, linearity and input matching Analog Integrated Circuits and Signal Processing Vol.73, pp.757-768, 2012.
9. Liang Wu, Hiu Fai Leung, Howard. C “Design and analysis of CMOS LNAs with Transformer feedback for WB input matching and noise cancellation”, IEEE Transactions on circuits and systems I. Vol 64, No 6, June 2022.
10. R. Dutta, P. Sharma, and S. Guha, “A SoC Based Low Power 8 – bit Flash ADC in 45nm CMOS Technology”, Proc. of the Int. Conf. on Advances in Electronics, Electrical and Computer Science Engineering — EEC 2012,

pp.60-64, 2012.

11. R. Dutta, T.D. Subash, and N. Paitya, “Improved DC Performance Analysis of a Novel Asymmetric Extended Source Tunnel FET (AES-TFET) for Fast Switching Application”, Silicon, Vol. 14, pp.3835–3841 (2022). https://doi.org/10.1007/s12633-021-01147-8
12. R. Dutta, M. Rahaman, A. Guha and N. Paitya, “Study of gate source-drain overlap/gate-channel underlap in Heteojunction (50nm Ge channel) n-Double Gate TFET for different κ -spacer”, 2019 Int. Conf. on Smart Systems and Inventive Technology (ICSSIT), Tirunelveli, India, 2019, pp. 672-676, doi: 10.1109/ICSSIT46314.2019.8987903.
13. Yun Chiu, “On the operation of CMOS Active cascade Gain stage”, Journal of computer and communication, Scientific Research. Vol 1, No.18, Nov 2013.
14. Sobhan Bhuiyan, M.A., M.R. Hossain, K.N. Minhad, F. Haque, and M.S.K. Hemel. 2022. CMOS Low-Dropout Voltage Regulator Design Trends: An Overview. *Electronics* 11 (2):193. doi: 10.3390/electronics11020193.
15. Sreenivasulu, V.B., and V. Narendar. 2022. Design insights of nano sheet FET and CMOS circuit applications at 5-nm technology node. *IEEE Transactions on Electron Devices* 69 (8):4115-4122. **doi:** 10.1109/TED.2022.3181575.
16. Ragonese, E. 2022. Design Techniques for Low-Voltage RF/mm-Wave Circuits in Nanometer CMOS Technologies. *Applied Sciences* 12 (4):2103. doi: 10.3390/app12042103.
17. Maji, K.B., B.P. De, R. Kar, D. Mandal, and S.P. Ghoshal. 2022. CMOS analog amplifier circuits design using seeker optimization algorithm. *IETE Journal of Research* 68 (2):1376-1385. doi:10.1080/03772063.2019.1649207.
18. A. Mamun, B. Sueoka, N. Allison, Y. Huang, and F. Zhao. 2022. Design and evaluation of in-plane silicon microneedles fabricated with post CMOS compatible processes. *Sensors and Actuators A: Physical* 336 (1):113407. doi:10.1016/j.sna.2022.113407.